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# Science Processing Hardware

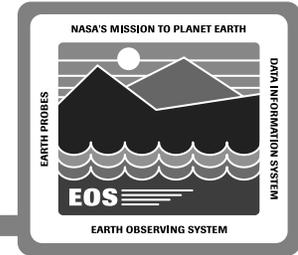
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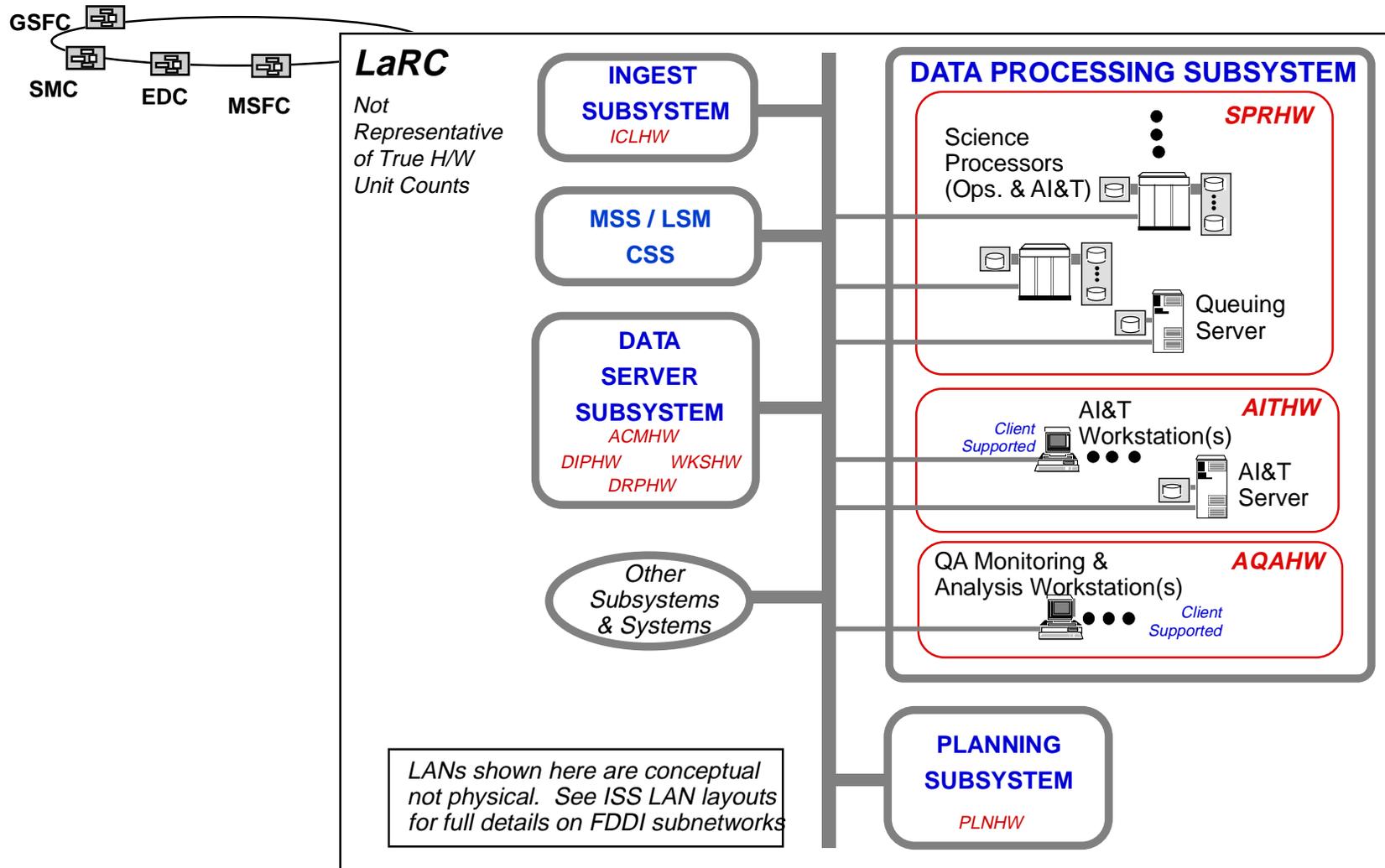
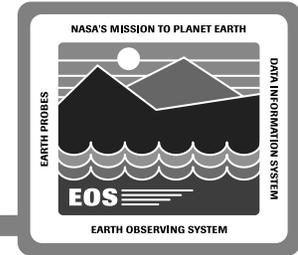
**ECS Release A SDPS/CSMS Critical Design Review  
August 16, 1995**

# Data Processing Overview

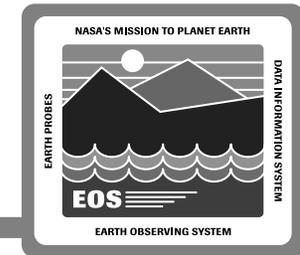


- **Data Processing overview given here focuses on the Science Processing HWCI (SPRHW), which:**
  - **Provides processing resources, system software, and COTS packages to support Science Processing, Algorithm Integration & Test, System Integration & Test and some capacity for Q/A**
- **Focus for Release A:**
  - **Reuse/incorporation of “lr1” configurations**
  - **Release A TRMM operations support at LaRC and MSFC (plus additional AM-1 AI&T support)**
  - **AI&T Support at GSFC and EDC**
  - **“Look Ahead” to Release B for scalability and evolvability**
  - **Address DAAC specific needs**

# SPRHW Within The Data Processing Subsystem

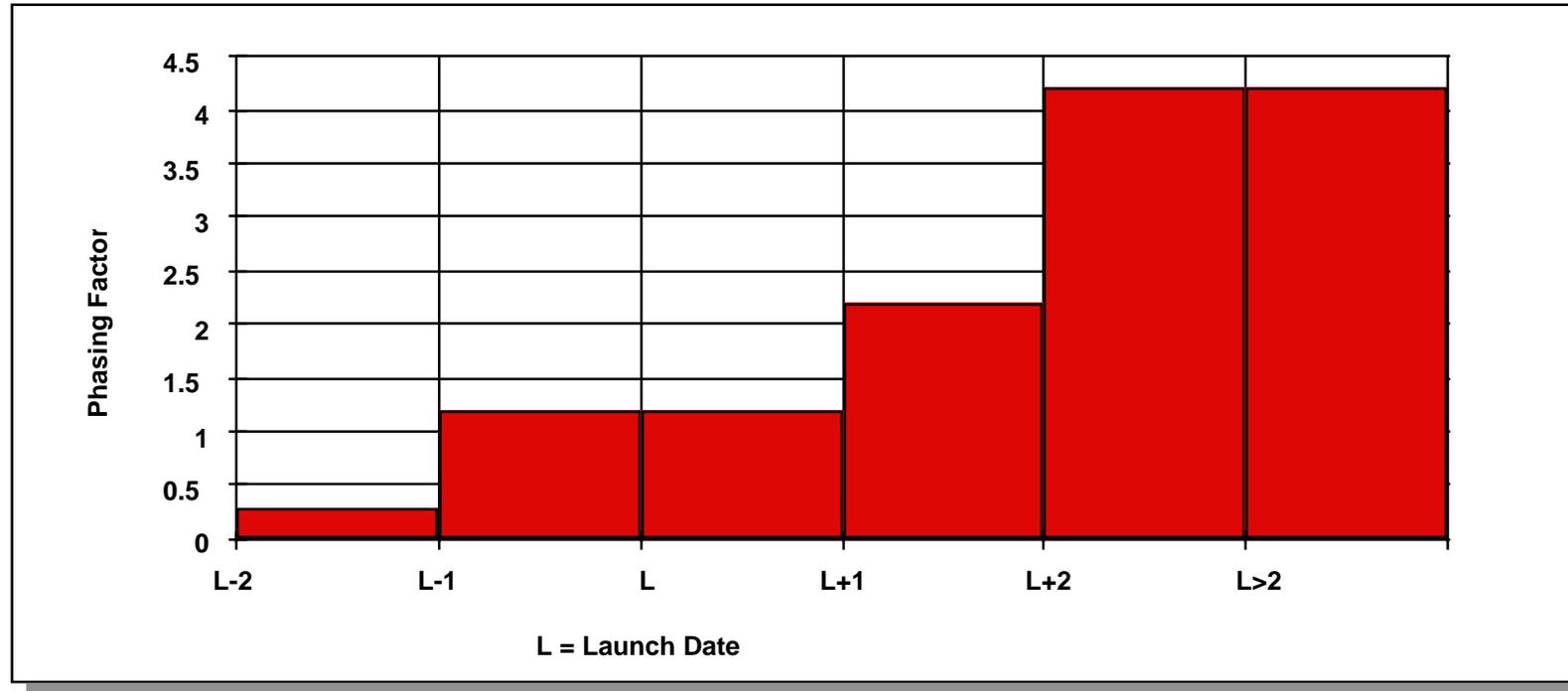
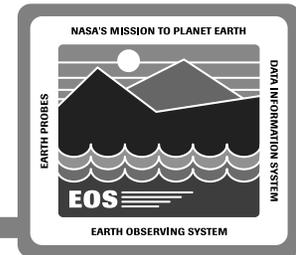


# SPRHW Configuration and Sizing Drivers



- **TRMM Processing Operations Drivers for LaRC and MSFC**
  - Operations hours (LaRC: “16x7,” “MSFC: 8x7”)
  - GSFC and EDC Processing for AI&T (Ir1 Follow-on Configurations)
- **ECS CDR Technical Baselines: June ‘95 AND Jan. ‘95**
- **AHWGP data is part of the CDR Technical Baseline:**
  - Processing, disk storage, I/O bandwidth, PGE activations
  - Derived “Peaks” From Dynamic Simulation
    - Simulation based on AHWGP inputs
- **ESDIS provided capacity Phasing Factors**
- **Separation of AI&T environment from operations environment**
  - Algorithm development, integration and maintenance
  - Provision for backup and failsoft processing requirements
- **Scalability and evolvability to Release B and beyond**
- **Production Queuing Server configuration driven by Planning Design**

# ESDIS Phasing Factors



## •0.3 X starting at L-2 years

- X is defined as at-launch processing estimate for pre-launch AI & T

## •1.2 X starting at L-1 years

- X is defined as at-launch processing estimate for pre-launch AI & T and systems I & T

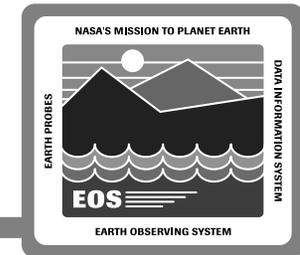
## •2.2 X starting at L+1 years

- X is defined as quarterly processing estimate for post-launch period

## •4.2 X starting starting at L+2 years

- X is defined as quarterly processing estimate for post-launch period

# Processing Design Rationale for CDR Builds on PDR Analysis



## Hardware Recommendation

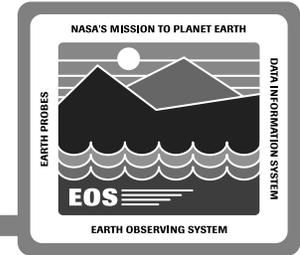
- **Static and Dynamic Analysis of AHWGP data**
  - **Dynamic: resource constrained discrete event simulation**
  - **Static: spreadsheet based analysis**
  - **Both analysis used for Release A, static used for Release B**
- **Trade Studies**
  - **Distributed and Parallel Processing (ref #: 440-TP-008-001)**
  - **Platform Families (ref #: 440-TP-007-001)**
  - **Production Topology (ref #: 440-TP-006-001)**
- **Mission Suitability Factors**
- **Price/performance Tradeoffs Re-examined**

## Design Supports:

- **Phased procurement**
- **Heterogeneous architectures (Uniprocessor & SMP)**

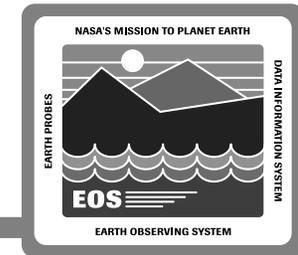
# Sample Dynamic Model Results - LaRC Disk Utilization

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**Not available electronically.**

# Processing Capacities for the DAACs at Release A (SPRHW)



DAAC	Required Phased Capacity*				Provided Capacity				
	Timeframe	MFLOPs	I/O	Disk Volume	Platform	MFLOPs	I/O Bandwidth	Disk Volume	RAM
LaRC	Ir1	1,100	25 MB/sec	30 GB	SMP (4 CPU)	1,200	320 MB/sec	68.8 GB	.5 GB
	TRMM Ops.	+5,632	+25 MB/sec	+5 GB	+SMP (20 CPU)	+6,000	+320 MB/sec	43 GB	+1.5 GB
	AM-1 AI&T	2,680	(TBR IDR)	30 GB	SMP (10 CPU)	3,000	320 MB/sec	43 GB	.5 GB
MSFC	Ir1	10	25 MB/sec	5 GB	Uniproc. WS	125	100 MB/sec	6 GB	256 MB
	TRMM Ops.	11	No Change	5 GB	+Uniproc. WS	+125	+100 MB/sec	6 GB	+256 MB
EDC	Ir1	120	25 MB/sec	35 GB	SMP (2 CPU)	600	320 MB/sec	43 GB	256 MB
	AM-1 AI&T	+966	+156 MB/sec	+35 GB	+ SMP (2 CPU)	+600	+320 MB/sec	+43 GB	+256 MB
GSFC	Ir1	2,150	+250 MB/sec	75 GB	SMP (6 CPU)	1,800	640 MB/sec	68.8 GB	2 GB
	AM-1 AI&T	+1,315	No Change	+35 GB	+6 CPU	+1,800	No Change	64.5 GB	No Chg.

## TABLE NOTES

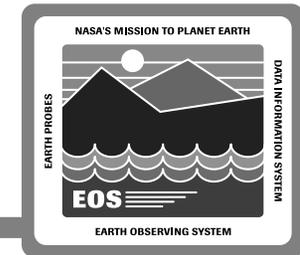
- Additional .9x capacity for AM-1 processing at launch minus 1 year (June '97) is delivered as part of Release B, and is therefore not shown here.\*
- Queuing Server configuration is equivalent to the Planning Server, & not shown here.
- "TRMM Ops." is @ PEAK MFLOPS, rest is nominal (static summation)
- AI&T disk: .3x phasing of at launch value (2 day's worth )
- AI&T I/O: .25x of launch requirement, phased to .3x
- Non-Ir1 RAM configurations under refinement (joint analysis)
- Provided capacity disk volumes, for RAID, include parity disk volumes

## Shading:

TRMM Ops. Sites

AI&T Only Sites

# Processing Architecture Recommendations for the Sites



**PDR recommendations for TRMM sites are refined in terms of capacity:**

- **MSFC TRMM LIS requirements for the TRMM mission require “Uni-processor” class hardware (unchanged since PDR)**
- **LaRC TRMM CERES configuration recommendation based on use of SMP class hardware (unchanged since PDR)**

**AI&T configurations for GSFC and EDC based on Ir1 use of SMPs:**

- **Static analysis of AM-1 AI&T and Release B requirements**
- **Phased capacities, with configurations adjusted per needs of teams and DAACs**

***Site configurations detailed further in DAAC Specific Poster Sessions***