

# IDR RID Report

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Originator Ben Jai

Phone No (818)354-9891

Organization JPL DAAC

E Mail Address bhj@seawind.jpl.nasa.gov

Document Release B JPL PO.DAAC Design Specification

RID ID	IDR	13
Review	IDR	
Originator Ref		bhj02
Priority	2	

Section Section 3.4

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Figure Table N/A

Category Name Hardware

Actionee ECS

Sub Category

Subject JPL DAAC processing and archive hardware

## Description of Problem or Suggestion:

Because the baseline document, Technical Baseline, August 1995, does not have correct information, the configuration presented in this document may not be correct either. Please refer to my RID bhj01 for details.

## Originator's Recommendation

The author of this document should modify this document and and redistribute it.

GSFC Response by:

GSFC Response Date

HAIS Response by: R. Miller

HAIS Schedule 11/15/95

HAIS R. E. Armstrong

HAIS Response Date 12/4/95

The originator is correct, the August 1995 Technical Baseline does not accurately reflect JPL processing requirements, and this impacted the analysis presented in the Design Specification for JPL.

The revisions to the Technical Baseline to correctly reflect JPL requirements will be evaluated using static and dynamic modeling of ECS, and the results will be used to re-assess the hardware specification for JPL. This evaluation and re-assessment will be performed as part of the analysis leading to Release-B CDR, which will incorporate other anticipated changes to the Technical Baseline and, if appropriate, changes to the hardware baseline (principally faster processors).

The results of these efforts will be published in the CDR version of the Release-B JPL Design Specification.

Status **Closed**

Date Closed **12/12/95**

Sponsor **desJardins/Marinelli**

\*\*\*\*\* Attachment if any \*\*\*\*\*